

Conferences > Proceedings of IEEE East-West...

Extending fault periodicity table for testing faults in memories under 20nm

Publisher: IEEE

Cite This

Cite This

PDF

G. Harutyunyan ; S. Shoukourian ; V. Vardanian ; Y. Zorian All Authors

4 Paper Citations

270 Full Text Views

Export to

Collabratec

Alerts

Manage

Content Alerts

Add to Citation

Alerts

More Like This

State model for scheduling Built-in Self-Test and scrubbing in FPGA to maximize the system availability in space applications
India International Conference on Power Electronics 2010 (IICPE2010)
Published: 2011

A Fully Integrated Built-In Self-Test $\Sigma\Delta$ ADC Based on the Modified Controlled Sine-Wave Fitting Procedure
IEEE Transactions on Instrumentation and Measurement
Published: 2010

Show More

Abstract

Document Sections

1. Introduction

2. Fault and Test Algorithm Periodicity

3. Finfet-Specific Faults

4. Extending Fault Periodicity Table

5. Conclusions

Download PDF

Abstract:A new solution for building memory BIST infrastructure, based on rules of fault periodicity and regularity in test algorithms was introduced recently. These rules are rep... **View more**

Metadata
Abstract:
A new solution for building memory BIST infrastructure, based on rules of fault periodicity and regularity in test algorithms was introduced recently. These rules are represented in a form of a Fault Periodicity Table (FPT) considering both known and unknown memory faults in one table. Each column of FPT corresponds to a fault nature which can be associated with a variety of different test mechanisms while each row of FPT corresponds to a fault family determined by the complexity of fault sensitization. In this paper, application of the proposed methodology for description of memory faults in technologies below 20nm, including 16/14nm FinFET-based memories, is shown. Specifically, it is shown that all recently discovered FinFET-specific faults successfully fit into FPT.

Published in: Proceedings of IEEE East-West Design & Test Symposium (EWDTS 2014)

Date of Conference: 26-29 Sept. 2014 **INSPEC Accession Number:** 14887812

Date Added to IEEE Xplore: 02 February 2015 **DOI:** 10.1109/EWDTS.2014.7027088

Publisher: IEEE

Electronic ISBN:978-1-4799-7630-0 **Conference Location:** Kiev, Ukraine

G. Harutyunyan
Synopsis

S. Shoukourian
Synopsys

V. Vardanian
Synopsys

Y. Zorian
Synopsys

 Contents

1. Introduction
Moder memory built-in self-test (BIST) controllers come either with
hardwired standard test algorithms or with a programmability option (see
[1]–[4]). Afterwards, solutions with programmability of separate test
mechanisms are proposed (e.g., [5], [6]).

Authors	^
G. Harutyunyan Synopsys	
S. Shoukourian Synopsys	
V. Vardanian Synopsys	
Y. Zorian Synopsys	
Figures	v
References	v
Citations	v
Keywords	v
Metrics	v

IEEE Personal Account	Purchase Details	Profile Information	Need Help?	Follow
CHANGE USERNAME/PASSWORD	PAYMENT OPTIONS	COMMUNICATIONS PREFERENCES	US & CANADA: +1 800 678 4333	f in t
	VIEW PURCHASED DOCUMENTS	PROFESSION AND EDUCATION	WORLDWIDE: +1 732 981 0060	
		TECHNICAL INTERESTS	CONTACT & SUPPORT	

About IEEE Xplore | Contact Us | Help | Accessibility | Terms of Use | Nondiscrimination Policy | Sitemap | Privacy & Opting Out of Cookies
A not-for-profit organization, IEEE is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity.
© Copyright 2021 IEEE - All rights reserved. Use of this web site signifies your agreement to the terms and conditions.

IEEE Account	Purchase Details	Profile Information	Need Help?
» Change Username/Password	» Payment Options	» Communications Preferences	» US & Canada: +1 800 678 4333
» Update Address	» Order History	» Profession and Education	» Worldwide: +1 732 981 0060
	» View Purchased Documents	» Technical Interests	» Contact & Support