Extending fault periodicity table for testing faults in memories under 20nm

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Abstract:
A new solution for building memory BIST infrastructure, based on rules of fault periodicity and regularity in test algorithms was introduced recently. These rules are represented in a form of a Fault Periodicity Table (FPT) considering both known and unknown memory faults in one table. Each column of FPT corresponds to a fault nature which can be associated with a variety of different test mechanisms while each row of FPT corresponds to a fault family determined by the complexity of fault sensitization. In this paper, application of the proposed methodology for description of memory faults in technologies below 20nm, including 16/14nm FinFET-based memories, is shown. Specifically, it is shown that all recently discovered FinFET-specific faults successfully fit into FPT.

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