Fault modeling and test algorithm creation strategy for FinFET-based memories

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Abstract:
FinFET transistors are playing an important role in modern technology that is rapidly growing. Embedded memories based on FinFET transistors lead to new defects that can require new embedded test and repair solution. To investigate FinFET-specific faults the existing models and detection techniques are not enough due to a special structure of FinFET transistors. This paper presents a new strategy for investigation of FinFET-specific faults. In addition to fault modeling, a new method is proposed for test algorithm synthesis. The proposed methodology is validated on several real FinFET-based embedded memory technologies. Moreover, new faults are identified that are specific only to FinFETs.

Published in: 2014 IEEE 32nd VLSI Test Symposium (VTS)

Date of Conference: 13-17 April 2014 **INSPEC Accession Number:** 14330755

Date Added to IEEE *Xplore*: 22 May 2014 **DOI:** 10.1109/VTS.2014.6818747

Electronic ISBN:978-1-4799-2611-4 **Publisher:** IEEE

ISSN Information: **Conference Location:** Napa, CA, USA

Contents

Due to growing leakage and short-channel problems of conventional planar MOSFET transistors, it is not possible to continue with Moore's Law by further scaling down the feature sizes of these planar transistors. FinFET transistors have been introduced as an alternative solution to further shrink the technology. The term FinFET was first mentioned as early as in 1999 in [1] to describe the non-planar double-gate transistor, which was demonstrated as a possible replacement for conventional planar technology. Later FinFETs were used in many publications to describe transistors built with new non-planar multi-gate architecture (see [2]–[7]). The distinguishing characteristic of FinFET transistor is that conducting channel consists of thin vertical silicon “Fins” that are wrapped around by gate electrodes. This leads to better control of channel and better electrostatic properties as leakage current is diminished in the off state and short channel effects are reduced.

Authors

Figures

References

Citations

Keywords

Metrics