Fault collapsing is an approach to alleviate the difficulties connected with the development of test sets for digital circuits. Since it is well-known

(see e.g. [2]) that the generation of a test for a single stuck-at fault even

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Footnotes

for an input line of a combinational circuit is a very difficult problem, then any possible reduction for the number of faults needing development of test sets, is a great benefit. That is why many authors have done research on this topic and some algorithms were proposed for fault collapsing [3]-[5]. As a result, the number of lines needing development of test sets was reduced sometimes unit 0.50% of leven more. Most of the proposed approaches that were classified as structural and functional refer to structural one when the relations of equivalence and dominance were defined between faults on input and output lines of logical gates. An extension of those notions, namely functional equivalence and functional dominance were also defined between any lines in a digital circuit allowing increase the percentage of fault collapsing [3]-[5]. At the same time, functional fault collapsing is a more difficult approach requiring availability of fast commercial programs for test generation of all stuck-at faults on every line in the circuit.

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Figures	~
References	~
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Metrics	~
Footnotes	~

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